WHAT IS CLAIMED IS:

1. A voltage controlled oscillator, comprising:

a first MOS transistor one end of which is connected to a first power source and to the gate electrode of which voltage for controlling the oscillation frequency is applied;

an oscillator connected between the other end of the first MOS transistor and a second power source;

a first capacitative element connected to the oscillator in parallel; and

additive control means that controls the oscillation frequency of the oscillator separately from the first MOS transistor.

2. A voltage controlled oscillator according to Claim 1, wherein:

the additive control means controls the oscillation frequency of the oscillator by a 1-bit digital signal.

3. A voltage controlled oscillator according to Claim 1, wherein:

the additive control means is composed of a second capacitative element and a second MOS transistor respectively connected in series between one of signal nodes in the oscillator and the second power source.

4. A voltage controlled oscillator according to Claim 1, wherein:

the oscillator is provided with at least three inverters in each of which a P-channel MOS transistor and an N-channel MOS transistor are connected in series;

the output and the input of the inverters are sequentially connected; and

the output of any inverter in odd order except first one is connected to the input of the first inverter.

5. A voltage controlled oscillator according to Claim 1, wherein:

the oscillator is provided with three or more odd inverters in each of which a P-channel MOS transistor and an N-channel MOS transistor are connected in series;

the output and the input of the inverters are sequentially connected; and

the output of a last inverter is connected to the input of a first inverter.

6. A PLL circuit that generates an output signal having a phase following the phase of a periodic reference signal and having a frequency of predetermined integral times, comprising:

a voltage controlled oscillator for generating the output signal;

a frequency divider that divides the output of the voltage controlled oscillator;

a phase comparator that generates a phase detection signal for differentiating a lead or delay of the phase of the output of the frequency divider to the phase of the reference signal;

a frequency comparator that discriminates the occurrence of difference between the frequency of the reference signal and the frequency of an output signal from

the frequency divider and generates frequency difference discrimination output; and

a control circuit that generates an analog control signal in which voltage varies according to output from the phase comparator and the frequency comparator, wherein:

the voltage controlled oscillator is provided with a MOS transistor one end of which is connected to a first power source and to the gate electrode of which the analog control signal is input, an oscillator connected between the MOS transistor and a second power source and a capacitative element connected to the oscillator.

7. A PLL circuit according to Claim 6, wherein:

the control circuit controls the voltage of the analog control signal according to the output of the phase comparator and the frequency comparator every cycle corresponding to one cycle of the reference signal; and

the variation of the voltage of the analog control signal in one cycle corresponding to one detection of difference between frequencies by the frequency comparator is larger than the variation of the voltage of the analog control signal in one cycle based upon the result of comparison by the phase comparator.

8. A PLL circuit according to Claim 6, wherein:

the control circuit controls the voltage of the analog control signal according to output from the phase comparator and the frequency comparator every cycle corresponding to one cycle of the reference signal; and

circuit means for inhibiting the variation of voltage

based upon the result of comparison by the phase comparator in a cycle in which the variation of voltage corresponding to the detection of difference between frequencies by the frequency comparator is applied and the predetermined numbers of cycles following the cycle is provided.

9. A PLL circuit that generates an output signal having a phase following the phase of a periodic reference signal and having a frequency of predetermined integral times, comprising:

a voltage controlled oscillator for generating the output signal;

a frequency divider that divides the output of the voltage controlled oscillator;

a phase comparator that generates a phase detection signal for differentiating a lead or delay of the phase of the output of the frequency divider to the phase of the reference signal;

a frequency comparator that discriminates the occurrence of difference between the frequency of the reference signal and the frequency of an output signal from the frequency divider and generates discrimination output; and

a control circuit that generates an analog control signal according to the output of at least the frequency comparator, wherein:

the voltage controlled oscillator is provided with a MOS transistor one end of which is connected to a first power source and to the gate electrode of which the analog

control signal is input, an oscillator connected between the MOS transistor and a second power source, a capacitative element connected to the oscillator in parallel and additive control means that controls the oscillation frequency by a phase detection signal output from the phase comparator.

10. A semiconductor integrated circuit, comprising:

a voltage controlled oscillator;

clock drivers that distribute the output of the voltage controlled oscillator to each circuit;

a frequency divider that divides one of clocks distributed by the clock drivers;

a phase comparator that generates a phase detection signal for differentiating a lead or delay of the phase of the output of the frequency divider to the phase of a periodic reference signal;

a frequency comparator that discriminates the occurrence of difference between the frequency of the reference signal and the frequency of an output signal from the frequency divider and generates frequency difference discrimination output; and

a control circuit that generates an analog control signal in which voltage varies according to the output of the phase comparator and the frequency comparator, wherein:

the voltage controlled oscillator is provided with a MOS transistor one end of which is connected to a first power source and to the gate electrode of which the analog

control signal is input, an oscillator connected between the MOS transistor and a second power source and a capacitative element connected to the oscillator in parallel.